REMARKS

The courtesy of Examiner Huisman in granting the interview of February 23, 2006, and the helpful comments proffered at that time is acknowledged with appreciation. Claims 1, 10 and 19 have been amended. Now in the application are Claims 1-20 of which Claims 1, 10 and 19 are independent. The following comments address all stated grounds of rejection and place the presently pending claims, as identified above, in condition for allowance.

I. Amended Claims 1, 10 and 19

Amended Claim 1 is directed to a method for managing a number of physical registers using a first structure, a second structure and a third structure. The first structure holds information identifying available physical registers that are free to be assigned as a destination operand for instructions. A physical register assignment is stored in the second structure noting that a selected physical registers is assigned as a destination operand for the architectural register of a selected instruction. The physical register assignment of the selected physical register is transferred from the second structure to the third structure after retirement of the selected instruction. The claimed invention further provides the steps of assigning said architectural register as a destination operand for a subsequent instruction, and prior to the retirement of said subsequent instruction, transferring information identifying said selected physical register as available from said third structure to said first structure. Claim 10 is another method claim reciting similar limitations, and claim 19 is a system claim that recites similar limitations as claim 1.

Yeager fails to disclose, teach or suggest the steps assigning said architectural register as a destination operand for a subsequent instruction, and prior to the retirement of said subsequent instruction, transferring information identifying said selected physical register as available from said third structure to said first structure, as required by amended Claims 1 and 10. As distinguished from the present invention, Yeager discloses that the old physical destination is moved from the active list to the free list upon graduation of a subsequent instruction, not upon an assignment of an architectural register as a destination operand for a subsequent instruction. Hence, the present invention increases the number of free physical registers available in a shorter

time period as compared to Yeager, and thus increases processing capacity of an associated micro-processor. More specifically, Yeager teaches that after a physical register (i.e., first physical register) is output from a free list and until it is written with a result from a corresponding instruction (i.e., first instruction), the physical register is "busy". If a subsequent instruction needs the values of this physical register (i.e., first physical register), such an instruction must wait until the register is written. After being written, the register (i.e., first physical register) is "ready", and its value is never changed. When a subsequent instruction (i.e., second instruction) changes the corresponding logical register associated with the first physical register to a second physical register, the result will be written into a new physical register (i.e., second physical register). When this subsequent instruction graduates, the old value is no longer needed, and the old physical register (i.e., first physical register) becomes "free" for re-use. Thus, physical registers have unambiguous values. *See*, Yeager Col. 7 50-63 (Emphasis Added).

As discussed above, Applicants assert Yeager teaches moving old physical destinations to the free list from the active list upon graduation of a subsequent instruction, not upon assignment of an architectural register for a subsequent instruction, which is significantly different in terms of structure, function and operation between Applicants' claimed invention and the invention taught by Yeager. Therefore, Yeager's step of retiring the second instruction as a prerequisite to moving a physical register from the active to the free list teaches away from transferring information identifying a physical register as available from the third structure to the first structure when the architectural register associated with the physical register is assigned as a destination operand for a subsequent instruction.

The arguments for amended Claim 19 parallel the above, and therefore, Yeager neither discloses, nor teaches, nor suggests all of the patentable features of amended Claim 19.

In light of the arguments set forth above, Applicants submit that the Yeager reference fails to disclose all of the elements of claims 1, 10 and 19. Claims 2-3 and 5-8 depend on claim 1 and therefore incorporate all the patentable features of claim 1. Claims 11-12 and 14-17 depend on 10 and therefore incorporate all the patentable features of claim 10. Claim 20 depends on Claim 19, and therefore incorporates all of the patentable features of Claim 20.

Application No.: 09/874173 Docket No.: SMQ-043RCE2 (P5215)

Applicants therefore request the Examiner to reconsider and withdraw the rejection of Claims 1-20 under 35 U.S.C. § 102 and 35 U.S.C. § 103.

II. Conclusion

In view of the remarks set forth above, Applicants contends that Claims 1-20 presently pending in this application are patentable and in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

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Respectfully submitted,

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